REMARKS

The above Amendments and these Remarks are in reply to the Office Action mailed February 25, 2004. Claims 1-51 are pending in the application. Applicant asserts that claims 1-51 are in condition for allowance and respectfully requests reconsideration of these claims. Applicant's arguments set forth below are supported by the *Isles Declaration* and the *Murgai Declaration*. References to portions of the *Isles Declaration* and the *Murgai declaration* are provided at the end of the appropriate paragraphs below.

I. Interview June 2, 2004

An interview was conducted between Applicant's representative and the Examiner on June 2, 2004. Claim 1 was discussed. The cited references: Weems, Charles C. Jr. "CmpSci 535 Notes from Lecture 9: Memory Hierarchy and Caching, 1996 ("*Weems*"); and Murgai, R. et al., *Logic Synthesis for Programmable Gate Arrays*, 27th ACM/IEEE Design Automation Conference, 1990 ("*Murgai*") were discussed. A first proposed amendment of claim 1 to recite "replacing a portion of a description of the electronic design relating to the physical memory with the lookup table, wherein the lookup table represents the physical memory," was discussed. The Examiner indicated that the proposed amendment was ambiguous and that a further search and consideration of *Murgai* would need to be undertaken if the amendment were submitted.

A second proposed amendment of claim 1 to recite "wherein the lookup table is used in a description of the electronic design to represent the physical memory and the lookup table is not the physical memory," was discussed. The Examiner indicated that a comma was needed after "physical memory" and that a further search and consideration of *Murgai* would need to be undertaken if the amendment were submitted.

II. Rejection of Claims 1-11, 23, 29-31, 45-47, and 50-51 under 35 U.S.C. §112, second paragraph

Claims 1, 23, and 29 were rejected for including the indefinite claim limitation, "... wherein the lookup table is used to represent the physical memory with a description of the electronic design." The rejected language has been removed from each of these claims.

Claim 1 now recites the additional functional step replacing a portion of a description of the electronic circuit design with the lookup table, wherein the portion of the description relates to the physical memory, and wherein the lookup table in the description represents the physical memory.

Applicant respectfully submits that the lack of clarity noted by the Examiner has been addressed by the segmented wherein clauses and that claims 1-11 and 45-47 are now definite and patentable under §112, second paragraph.

Claim 23 now recites "wherein the hardware description language of the lookup table represents the physical memory of the electronic circuit design." Applicant respectfully submits that the lack of clarity noted by the Examiner has been addressed by the cited wherein clause and that claims 23 and 50 are now definite and patentable under §112, second paragraph.

Claim 29 now recites "replacing a portion of a description of the electronic circuit design with the lookup table, wherein the portion of the description relates to the physical memory, and wherein the lookup table in the description represents the physical memory." Applicant respectfully submits that the lack of clarity noted by the Examiner has been addressed by the segmented wherein clauses and that claims 29-31 and 51 are now definite and patentable under §112, second paragraph.

Claims 12-13, and 48 were rejected for including the indefinite claim limitation, "... wherein the lookup table is used to represent the combinational block with a description of the electronic design." The rejected language has been removed from claim 12 which now recites, "replacing a portion of a description of the electronic circuit design with the lookup table, wherein the portion of the description relates to the uninterpreted combinational block, and wherein the lookup table in the description represents the uninterpreted combinational block." It is respectfully submitted that the lack of clarity noted by the Examiner has been addressed by the amended language and claims 12-13 and 48 are patentable under §112, second paragraph.

Claims 14-22, 34-41, and 49 were rejected for including the indefinite claim limitation "...wherien the memory model is used to represent the physical memory with a description of the electronic design." The rejected language has been removed from these claims.

Claims 14 and 34 now recite "replacing a portion of a description of the electronic circuit design with the memory model, wherein the portion of the electronic circuit design relates to the physical memory, and wherein the memory model in the description represents the physical memory." It is respectfully submitted that the lack of clarity noted by the Examiner has been addressed by the segmented wherein clauses included in the amended limitations and that claims 14-22, 34-41, and 49 are patentable under §112, second paragraph.

III. Technology at Issue and Summary of Invention

Embodiments of Applicant's invention relate to electronic design automated (EDA) systems and memory models that can be used with such design systems. The design process for integrated circuits typically involves multiple transformations of a design from an initial idea to a functional, manufacturable product. A chip architect or designer begins with a design idea and then generates a corresponding behavioral definition of the design. The behavioral design results in a flow chart or a flow graph using which the designer can design the system data path and the registers and logic units necessary for implementation of the design. After the designer designs buses for coordinating and controlling the movement of data between registers and logic units, the data registers, buses, logic units, and their controlling hardware are implemented using logic gates and flip-flops. The result of this design stage is a netlist of gates and flip-flops. The netlist can be used to create a simulation model of the design to verify the design before it is built. Once the design has been verified, the netlist can be used to provide the information needed by a routing software package to complete the actual design. The netlist of gates and flip-flops is thus transformed into a transistor list or layout and gates and flip-flops are replaced with their transistor equivalents or library cells. Timing and loading issues are also addressed during this cell and transistor selection process. Finally, the manufacturing process begins when the transistor list is implemented in a programmable logic device such as an FPGA or when the layout specification is used to generate masks for integrated circuit fabrication. *See generally*, Applicant's Specification, pp. 1-2 and *Isles Declaration*, ¶ 8.

EDA tools improve upon this design process by permitting electronic circuit designers to more quickly and inexpensively design and verify their designs. Figure 1 of Applicant's Specification illustrates a typical design approach using EDA tools. The designer initially supplies a logic synthesis tool 120 with a high level language description 110 of the design and the logic synthesis tool 120 reduces the high level language description 110 to a low level or gate level description 130 of the design. Finally, verification or simulation of the design is performed by an engine 140 using a set of properties 150 or behaviors as an input to determine whether, and to what extent, the design described by HDL description 110 satisfies the properties 150. The properties 150 are based on a functional specification for the design being verified or simulated. *See id.* at p. 2 and ¶ 9.

The design approach of Figure 1 has also been previously used to model, synthesize, and verify memory circuit designs. However, prior art memory models suffered from two major disadvantages. First, they modeled every location of the memory even if only a subset of locations of the memory were needed to perform the verification. For example, consider the case of a electronic

design description that contains a RAM with 1024 memory locations along with one read port and one write port. If on each cycle, one memory read operation and one memory write operation can occur simultaneously, and the designer would like to model the behavior of the RAM over five clock cycles, then only 10 locations (2 memory locations per clock cycle * 5 clock cycles) need to be modeled, not 1024 as required by these prior art memory models. Verifying or simulating a memory model that contains all 1024 locations is inefficient and wastes valuable resources. Second, memory models from one EDA vendor could typically only be used with simulation or verification engines from the same vendor. In other words, the choice to use a particular prior art memory model necessitated a particular verification or simulation engine. This lack of interoperability greatly limits the utility of prior art memory models. *See generally*, Applicant's Specification, pp. 3-4 and *Isles Declaration*, ¶ 10.

Embodiments of Applicant's invention provide a solution to the problems identified above by modeling a physical memory in a lookup table that can then be used in a description of the electronic design to represent the physical memory during the design and verification process. The lookup table is developed and used with a description of an electronic circuit design in order to model the circuit prior to the development of any actual physical memory or circuit and prior to completing an actual physical design. In one embodiment for example, an EDA tool that can exclusively be software, is used to model, synthesize, verify and/or simulate a circuit design model described only in a software language such as hardware description language (HDL) or by a gate level netlist. No hardware is needed to perform the modeling or to describe the electronic circuit design. Accordingly, the EDA tools permit "designers to more quickly and inexpensively design and verify their designs" before a routing software package is used to complete an actual physical design. *See generally*, Applicant's Specification, pp. 1-5.

Similarly, embodiments of Applicant's invention provide a solution to the problem of modeling an uninterpreted combinational block using a lookup table that can then be used in a description of the electronic design to represent the combinational block during the design and verification process. An uninterpreted combinational block (some times referred to as a "black box") is a portion of an electronic circuit description that represents a combinational block whose input and outputs are given but whose actual functionality is not defined. The lookup table is developed and used with a description of an electronic circuit design in order to model the circuit prior to the development of any actual combinational block or circuit and prior to completing an actual physical design. In one embodiment for example, an EDA tool that can exclusively be software, is used to

model, synthesize, verify and/or simulate a circuit design model described only in a software language such as hardware description language (HDL) or by a gate level netlist. No hardware is needed to perform the modeling or to describe the electronic circuit design. Accordingly, the EDA tools permit "designers to more quickly and inexpensively design and verify their designs" before a routing software package is used to complete an actual physical design. *See* generally, Applicant's Specification, pp. 1-5.

IV. Rejection of Claims under 35 U.S.C. §103(a)

Claims 1-22 and 29-51 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Weems, Charles C. Jr. "CmpSci 535 Notes from Lecture 9: Memory Hierarchy and Caching, 1996 ("*Weems*") in view of Murgai, R. et al., *Logic Synthesis for Programmable Gate Arrays*, 27th ACM/IEEE Design Automation Conference, 1991 ("*Murgai*"). Because there is no motivation or suggestion in the relevant field of endeavor whereby one of ordinary skill in the art would make the combination suggested by the Examiner, and furthermore, because even if the suggested combination is made, the resulting combination fails to teach or suggest each of the limitations of amended claims 1-22 and 29-51, Applicant asserts that these claims are patentable over the art of record.

Claim 23 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Bayoumi, M. et al., *A Look-Up Table VLSI Design Methodology for RNS Structures Used in DSP Applications*, IEEE Transactions on Circuits and Systems, Vol. 34, Issue 6, June 1997, pp. 604-616 ("*Bayoumi*") in view of *Murgai*, and claims 24 -28 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Bayoumi* in view of *Murgai*, and further in view of *Weems*. Because there is no motivation or suggestion in the relevant field of endeavor whereby one of ordinary skill in the art would make the combinations suggested by the Examiner, and furthermore, because even if the suggested combinations are made, the resulting combinations fail to teach or suggest each of the limitations of amended claims 23-28, Applicant asserts that these claims are patentable over the art of record.

A. Lack of Evidence to Support a rejection under 35 U.S.C. §103(a)

Because the Examiner has presented no evidence of a motivation or suggestion to combine the cited references to arrive at Applicant's claimed invention, and furthermore, because Applicant has provided evidence that such motivation or suggestion does not in fact exist, Applicant asserts that claims 1-51 are patentable over the cited art.

The teachings of *Weems* and *Murgai* and *Bayoumi* and *Murgai* have been combined by the Examiner on the sole basis of a quoted passage from *Murgai* that simply recites, "[p]rogrammable devices (PD's) are devices that can be programmed by the user to implement a logic function. Because of short turnaround time, they are becoming increasingly important for rapid system prototyping. In addition, they have a low cost of manufacturing and are fully testable. For short turnaround, it is necessary to have automatic tools that take a 'high-level description' (like equations or a VHDL description) of a circuit and synthesize onto these architectures." *See Office Action*, p. 6.

It is respectfully submitted that the mere quotation of a passage from *Murgai* which states what a programmable device is, their importance for system prototyping, and the need for automatic tools in the synthesis thereof is not evidence of a motivation or suggestion to combine such teachings with teachings in the different fields of endeavor of computer architecture to which *Weems* is directed and integrated circuit design methodologies to which *Bayoumi* is directed. Furthermore, the quotation of the cited passage provides no evidence of a motivation or suggestion to combine such teachings in different fields of endeavor to somehow arrive at the invention as recited in Applicant's claims, which is directed to modeling memory operations or uninterpreted combinational blocks during the simulation and verification stage of electronic circuit design.

In contrast to the Examiner's unsubstantiated assertion, Applicant has provided evidence in the form of the accompanying *Isles Declaration* that no such motivation or suggestion exists. The *Isles Declaration* details the teachings of each reference and explains the disparate fields of endeavor to which each is directed. The *Isles Declaration* further details how Applicant's claimed invention is in a different field of endeavor from each of the cited references. Finally, the *Isles Declaration* explains that one of ordinary skill in the art of electrical engineering would not be motivated to combine teachings in such disparate fields to arrive at an invention in yet a further different field. *See Isles Declaration*, ¶¶ 11-18.

Because the Examiner has provided no evidence of a motivation or suggestion to combine the cited references and because Applicant has provided evidence that no such motivation or suggestion exists, it is respectfully submitted that claims 1-51 are patentable over the cited art under 35 U.S.C. § 103(a).

B. There is no Motivation or Suggestion to Combine the Cited References

It is respectfully submitted that there is no explicit or implicit suggestion in either reference, or an implicit motivation in the knowledge generally available to one of ordinary skill in the art, whereby one would be led to combine such disparate references as suggested by the Examiner.

The Examiner has combined *Weems's* disclosure of memory hierarchy and caching in the field of computer architecture and *Murgai's* disclosure of logic synthesis of programmable gate arrays under the sole rationale that it would have been obvious to "modify the teachings of *Weems* with those of *Murgai* because 'Programmable devices (PD's) are devices that can be programmed by the user to implement a logic function. Because of short turnaround time, they are becoming increasingly important for rapid system prototyping. In addition, they have a low cost of manufacturing and are fully testable. For short turnaround time, it is necessary to have automatic tools that take a 'high-level description' (like equations of VHDL description) of a circuit and synthesize onto these architectures." *Office Action*, p. 6.

Applicant's claimed invention is directed to models of physical memory and uniterpreted combinational blocks used in the simulation and verification of electronic circuit designs. The references cited by the Examiner, however, are directed at some level to actual physical structures such as physical memory and its layout, the use of physical memory in computers, or the physical design and layout of circuits. These reference are in distinct fields of endeavor from one another, as well as in distinct fields of endeavor from Applicant's claimed invention. *Weems* is directed to the temporary storage of data in a computer while *Murgai* is directed to taking an already developed description and synthesizing it onto a physical architecture. From the perspective of one of ordinary skill in the field of electrical engineering and computer science, the work of *Weems* and *Murgai* are disparate and are related only in the very loose sense that they concern some phase of the design, development, and physical implementation of electronic systems. While each reference may use some variant of the term "look-up table," the teachings of each reference cannot be easily extended or applied to solve the problems of the other reference or of Applicant's claimed invention. *See Isles Declaration*, ¶¶ 11-15.

Weems, for example, is directed to the field of Computer Architecture, which is considered by those of ordinary skill in the relevant arts as orthogonal to the field of electronic design automation altogether. *Weems* is concerned with designing memory systems for computers that will maximize the performance (in terms of the speed of performing memory read and write operations) of the physical implementation of the computer memory while minimizing the cost of manufacturing the physical

implementation of the computer memory. *Weems* achieves this goal by way of using memory hierarchies. Such hierarchies include cache memories, which are small, fast and relatively expensive memories systems that act as an intermediaries between the computer's main processor and the large, slow and relatively inexpensive main memories (such as RAMs) which are found in modern computer systems. *See Weems*, pp. 2-7. Weems discusses techniques for copying data form the slower, larger, memories to the smaller, faster cache memories (and vise-versa). *See id.* He also shows how such systems and related techniques can be implemented using look up tables and other structures. *See id.* at pp. 10-11. Absolutely nowhere in *Weems* does the author discuss approaches of how electronic design descriptions that contain memories (such as RAMs) can be modeled (by using lookup tables or any other method) for efficient simulation and verification using an EDA tool. *See Isles Declaration*, ¶¶ 11-12.

In contrast to both *Weems* and Applicant's claimed invention, *Murgai* is directed to the field of study and art called logic synthesis (which is considered part of the EDA field, but still separate from simulation or verification of electronic circuit descriptions). In particular, *Murgai* is not concerned with the modeling of memories, but rather, the actual physical synthesis of a "'high-level description' of a combinational circuit (like equations or a VHDL description) onto a programmable gate array architecture (which is physically realized using an array of table lookups or multiplexors). *Murgai*, 1. Introduction. Absolutely no where does Murgai discuss approaches of how electronic design descriptions that contain memories (such as RAMs) can be modeled (by using lookup tables or any other method) for efficient verification using an EDA tool. *See Isles Declaration*, ¶¶ 13; *see also Murgai Declaration*, ¶¶ 7-14.

Because each reference is in such a distinct field of endeavor and makes no mention of any remote applicability to the field of the other, there is no explicit or implicit motivation within either reference to combine them as suggested by the Examiner. There is nothing in *Weems* that would suggest taking such a data storage technique and combining it with techniques for realizing a physical implementation of a circuit description using a programmable gate array. Likewise, *Murgai* is directed to synthesizing circuit level descriptions onto PGA's. There is nothing in *Murgai* to suggest the expansion of the described techniques into a computing environment where cache memory is used to increase performance in data retrieval. Furthermore, one of ordinary skill in the art would find no such motivation or suggestion from the knowledge generally available in the relevant fields of art to make such a combination. Additionally, because each reference is in a disparate field from that of Applicant's claimed invention, there is no motivation or suggestion in the references or in the field of

art to make such a proposed combination to arrive at Applicant's claimed invention. *See Isles Declaration*, ¶¶ 14-15; *see also Murgai Declaration*, ¶¶ 7-14.

Because there is no motivation or suggestion to combine *Murgai* and *Weems* as suggested by the Examiner, Applicant respectfully submits that claims 1-22 and 29-51 are patentable over the cited art.

The Examiner has further combined *Murgai's* disclosure of logic synthesis of programmable gate arrays with *Bayoumi's* disclosure of IC design methodology under the same rationale and quoting the same passage as set forth with respect to the combination of *Weems* and *Murgai*. Again, however, these references are in distinct fields of endeavor from one another as well as in distinct fields of endeavor from Applicant's claimed invention.

Murgai is directed to taking an already developed description and synthesizing it onto a physical architecture while *Bayoumi* is in yet another field, usually referred to as integrated circuit (IC) design. In the work that is cited, *Bayoumi* is specifically interested in methodologies for creating integrated circuits for digital signal processing architectures that use a special form of arithmetic, called the residue number system (RNS). *See Bayoumi*, p. 607. Bayoumi discusses how RN-systems have been shown to be suitable for the physical implementation using networks of look-up tables which are interconnected together on an integrated circuit. In particular, the disclosure is concerned with the methodology of choosing the size of each lookup table in terms of the number of bits involved, the area, width, timing delay, etc. of the physical implementation. *See id.* at pp. 604, 606-607, 610-611. While the terminology in *Bayoumi* is somewhat confusing, one of ordinary skill in the art would understand the term "memory module" to which *Bayoumi* refers as a storage array and supporting circuitry necessary to physically implement a look-up table on an integrated circuit. *See id.* at pp. 606-607. The term "memory model" would be understood to refer to a mathematical tool employed to help determine the best way (in terms of area and access time) to implement the lookup table on an integrated circuit. *See Bayoumi* at pp. 607-608; *See Isles Declaration* at ¶ 16.

Methods for how to model memory reads and writes or uninterpreted combinational blocks, for example, are never discussed and are not relevant to the disclosure in *Bayoumi*. *Bayoumi* is directed to a model that "simulates the physical layout of a memory module" such as a look-up table which "represents the basic building block unit of the RNS memory intensive architectures" addressed therein. Bayoumi, pp. 607-608. In *Bayoumi* the look-up table is the actual physical memory to be laid out on a chip, not a model (such as a software model) of a physical memory. Again, absolutely

nowhere does Bayoumi discuss approaches of how electronic design descriptions that contain memories (such as RAMs) can be modeled (by using lookup tables or any other method) for efficient verification using an EDA tool. *See Isles Declaration* at ¶ 17.

One of ordinary skill in the art would not be motivated or suggested to somehow combine the teachings directed to physical networks of lookup tables which are interconnected on an integrated circuit with teachings directed to the synthesis of high-level descriptions onto lookup table architectures. From the perspective of one of ordinary skill in the field of electrical engineering and computer science, the teachings of *Murgai* and *Bayoumi* are disparate and related only in the very loose sense that they concern some phase of the design, development, and physical implementation of electronic systems. Neither reference contains any disclosure relevant to models of physical memories. Each reference is in someway directed to the actual physical memory itself, either by way of a network of interconnected physical lookup tables or the synthesis of designs onto physical lookup tables. Nothing within either reference or the knowledge of those of ordinary skill in the art suggests anything relating to lookup tables which are models of physical memory used in electronic circuit design descriptions. *See Isles Declaration*, ¶ 18; *see also Murgai Declaration*, ¶¶ 7-14.

Because there is no motivation or suggestion to combine *Murgai* and *Bayoumi* as suggested by the Examiner, Applicant respectfully submits that claim 23, and by their dependency therefrom, claims 24-28, are patentable over the cited art.

C. The Combination of *Weems* and *Murgai* Fails to Teach or Suggest each of the Limitations of Claims 1-22 and 29-51

Claims 1-11 and 45-47

Novel features of Applicant's invention set forth above are embodied in claim 1 which, as amended, recites three steps for "modeling a physical memory for use in an electronic circuit design." In the first step, "a memory write operation of the electronic circuit design [is modeled] using a lookup table." In the second step, "a memory read operation of the electronic circuit design [is modeled] using the lookup table." The third step involves replacing "a portion of a description of the electronic circuit design with the lookup table." The replaced portion "relates to the physical memory" and "the lookup table in the description represents the physical memory."

It is submitted that even if *Weems* and *Murgai* are combined as suggested by the Examiner, the resulting combination fails to teach or suggest this method recited in claim 1. The combination of references fails to teach or suggest either of the following limitations:

modeling a memory write operation of the electronic circuit design using a lookup table;

modeling a memory read operation of the electronic circuit sign using the lookup table...

Weems's memory hierarchy and caching disclosure does not suggest such modeling of memory operations and does not discuss electronic circuit design as addressed in claim 1. *Weems* merely discloses storing data from a main memory in a smaller, faster, cache memory to increase memory access performance as is well known in the art. *Weems* teaches that because only a small amount of a memory space is accessed at any given time, values in that subset are copied "from slower memory to the small fast memory." *Weems*, p. 2. There is no modeling of a read or write operation, just the temporary storage of data in a secondary memory with a fast access time. *See Isles Declaration*, ¶¶ 20-21.

Furthermore, there is no disclosure relating to a "electronic circuit design" as recited in claim 1. Cache memory stores data and the process of storing such data does not entail modeling anything relating to an electronic circuit design. *Id.*

The Figure on p. 3 and accompanying text cited by the Examiner do not address "modeling a memory write [read] operation" or an "electronic circuit design," as recited in claim 1. The figure is merely a diagram of a cache that contains "lines of data, usually containing values from two or more consecutive addresses of main memory. *Weems*, p. 3. Each line has associated with it a tag that stores the high order bits of the addresses in the line." *Id.* There is no discussion relating to modeling memory read or write operations at all, much less in the context of "electronic circuit design[s]" as recited in claim 1. The text simply discusses the process of comparing the address of a memory reference with the tags in the cache to determine if the data is stored in the cache memory. For example, if "there is a match then the line of data is read from the cache and low order bits of the address select the appropriate word from the line to be passed to the CPU." *Id.*; *see also, Isles Declaration* ¶¶ 20-21.

Furthermore, pages 7-8 regarding "write" and "write buffer" as referenced by the Examiner similarly do not address modeling of memory operations or an electronic circuit design. *Weems* discloses two options for writing data to the cache memory. In write through, "we can write it to the cache and simultaneously write it in through to the main memory." *Weems*, p. 7 In write back, "we can write it to the cache and not write it back to the main memory until it is replaced." *Id.* There simply is no disclosure pertaining to modeling. With regards to the material under the heading "write buffer," *Weems* addresses the problem of the processor having to wait while data is written to main

memory by using a buffer. *Id.* at p. 8. The buffer is simply "a small set of registers" to which "data and its destination address are written ... where they waits for memory to become available so the data can actually be stored." *Id.* Clearly *Weems's* discussion relating to cache writing techniques and write buffers does not suggest "modeling a memory write [read] operation of the electronic circuit design using a lookup table." *Isles Declaration*, ¶¶ 20-21.

Murgai also fails to teach or suggest these limitations. *Murgai* is directed to logic synthesis onto programmable gate array architectures (PGA), not "modeling a memory write [read] operation of the electronic circuit design using a lookup table," as recited in claim 1. *Murgai* discusses "automatic tools that take a 'high level description' (like equations or a VHDL description) of a circuit and synthesize onto these [programmable device] architectures." *Murgai*, 1. Introduction. For example, PGA architectures "consist of repeated arrays of identical logic blocks" which are "a versatile configuration of logic elements which can be programmed by the user." *Id.* One category of logic blocks are "Table Look-Up (TLU)" which have a resulting TLU architecture. *Id.*; *see also Isles Declaration*, ¶¶ 22-23.

Murgai does not disclose modeling write or read operations using a look-up table. Rather, *Murgai* discloses that one type of physical architecture for programmable gate arrays are Table Look-Up. A write or read operation is not modeled using *Murgai's* Table Look-Up. The TLU is the actual architecture onto which a "high-level description" is to be synthesized. *Isles Declaration*, ¶¶ 22-23.

It is further submitted that the combination of references fails to teach or suggest the following limitation of claim 1:

> ... replacing a portion of a description of the electronic circuit design with the lookup table, wherein the portion of the description relates to the physical memory, and wherein the lookup table in the description represents the physical memory...

Weems does not address and is not related to electronic circuit design, descriptions of electronic circuit designs, or modeling read and write operations for electronic circuit designs. Accordingly, *Weems* fails to contain any teaching or suggestion of the above cited limitation of claim 1. *Isles Declaration*, ¶¶ 20-21.

The Examiner recognized that *Weems* fails to teach using a lookup table "to represent the physical memory with a description of the electronic design," and cited *Murgai* for the disclosure a similar limitation pending prior to the present amendment. It is respectfully submitted that *Murgai* fails to teach or suggest "replacing a portion of a description of the electronic circuit design with the

lookup table; wherein the portion of the description relates to the physical memory, and wherein the lookup table in the description represents the physical memory," as now recited in claim 1.

First, even if *Murgai* discloses that "equations or VHDL are used to 'model' the Table Look-Ups (TLU) used in the Programmable Gate Arrays (PGA)," as the Examiner concludes, the asserted disclosure does not teach or suggest "wherein the lookup table in the description represents the physical memory," as recited in claim 1. The Examiner asserts that *Murgai* teaches equations or VHDL that "are used to 'model' the Table Look-Ups." Although a table can be expressed in VHDL, claim 1 recites a table that "represents the physical memory." In claim 1, the table is the model, not what is modeled, as asserted by the Examiner. Therefore, even if *Murgai* teaches that "equations or VHDL are used to 'model' the Table Look-Ups (TLU) used in the Programmable Gate Arrays (PGA)," this is not a teaching or suggestion of the above-cited limitation of claim 1. *Isles Declaration*, ¶ 23; *Murgai Declaration*, ¶¶ 7-10.

Second, it is respectfully submitted that *Murgai* does not in fact disclose "that equations or VHDL are used to 'model' the Table Look-Ups (TLU) used in the Programmable Gate Arrays (PGA)." *Murgai* teaches the use of automatic tools that synthesize high-level descriptions of a circuit onto PGA architectures which can include Table-Look-Up (TLU) in one category. The TLU is the physical architecture of the PLA onto which the description is being synthesized. The TLU is not somehow placed into the description. It is the actual physical architecture. The description is synthesized onto the TLU architecture, not modified to include the TLU. Accordingly, nowhere does *Murgai* teach that the equations or a VHDL description are used to model these Table Look-Ups. *Murgai's* only teaching is that these equations or VHDL descriptions are "synthesize[d] onto these architectures" which can include Table Look-Up. *Murgai*, 1. Introduction; *Isles Declaration*, ¶¶ 22-23; *Murgai Declaration*, ¶¶ 7-15.

Thus, even if *Weems* and *Murgai* are combined as suggested by the Examiner, the resulting combination fails to teach or suggest each limitation of claim 1. Accordingly, it is respectfully submitted that claim 1 is patentable over the cited art. Claims 2-11 and 45-47 each ultimately depend from claim 1 and should be patentable for at least the same reasons.

Claims 12-13 and 48

Even if the references are combined as suggested by the Examiner, the combination fails to teach or suggest all of the limitations of claims 12-13 and 48. Accordingly, Applicant asserts that claims 12-13 and 48 are patentable over the cited art.

The combination of *Weems* and *Murgai* fails to teach or suggest the following limitation of claim 1:

> ... replacing a portion of a description of the electronic circuit design with the lookup table, wherein the portion of the description relates to the uninterpreted combinational block, and wherein the lookup table in the description represents the uninterpreted combinational block.

As set forth with respect to claim 1, *Weems* is directed to a cache memory system that utilizes a smaller, faster memory to increase memory access performance. There is no disclosure within *Weems* of modeling memory read or write operations of an electronic circuit design at all. Similarly, there is no teaching or suggestion of a lookup table that "represents the uninterpreted combinational block." *Weems's* description of write caching only relates to techniques for writing data to and reading data from a cache memory which is a physical memory structure. *Isles Declaration*, ¶¶ 20-21, 25.

The additional portions of *Weems* cited in the rejection of claim 12 relating to "paging" and the "presence bit" on p. 11 further do not suggest such a limitation. The lookup table disclosed by *Weems* in the section relating to "paging" is simply used to perform a mapping from a virtual address space to a physical address space. Virtual memory is defined by *Weems* as a "mapping from a virtual address space to a physical address space," or a "mapping from a name space to an address space." *Weems* at p. 10. "In order to perform the mapping function, a table lookup is performed." *Weems*. at p. 11. The lookup table of *Weems* is used for performing a mapping function. It in no way "represents the uninterpreted combinational block," as recited in claim 12. *Isles Declaration*, ¶¶ 20-21, 25.

It was shown with respect to claim 1 that *Weems* fails to disclose "replacing a portion of a description of the electronic circuit design with the lookup table, wherein the portion of the description relates to the physical memory, and wherein the lookup table in the description represents the physical memory." Similarly, *Weems* contains no suggestion for "replacing a portion of a description of the electronic circuit design with the lookup table, wherein the portion of the description relates to the uninterpreted combinational block, and wherein the lookup table in the description represents the uninterpreted combinational block." *Weems's* disclosure does not relate to electronic circuit design and therefore, does not address using a lookup table in such a design. The lookup table of *Weems* is simply used "to perform the mapping function" from virtual address space to physical address space. There is nothing to suggest "replacing a portion of a description of the

electronic circuit design with the lookup table," as recited in claim 12. *Isles Declaration*, ¶¶ 20-21, 25.

Murgai fails to remedy the identified deficiencies of *Weems*. As set forth with respect to claim 1, the Table Look-Up (TLU) architecture in *Murgai* is a category of physical block structures. *Murgai's* disclosure pertains to synthesizing a high-level description onto these TLU architectures. The TLU is not a model and is not used to represent an uninterpreted combinational block in an electronic circuit design. Rather, the description of a circuit design is synthesized onto this physical TLU architecture. *Isles Declaration*, ¶¶ 22-23, 26; *Murgai Declaration*, ¶¶ 7-14, 16.

Thus, even if *Weems* and *Murgai* are combined as suggested by the Examiner, the resulting combination fails to teach or suggest each limitation of claim 12. Accordingly, it is respectfully submitted that claim 12 is patentable over the cited art. Claims 13 and 48 depend from claim 12 and should be patentable for at least the same reasons.

Claims 14-22 and 49

Even if the references are combined as suggested by the Examiner, the combination fails to teach or suggest all of the limitations of claims 14-22 and 49. Accordingly, Applicant asserts that claims 14-22 and 49 are patentable over the cited art.

As set forth with respect to claim 1, the combination of *Weems* and *Murgai* fails to teach or suggest "modeling a memory write [read] operation of the electronic circuit design using a lookup table." Specifically, it was shown that the combination fails to suggest modeling memory write or read operations of electronic circuit designs in any fashion. Accordingly, at least for the same reasons set forth therein, it is submitted that the combination of references fails to teach or suggest, "modeling a memory write operation of the electronic circuit design in a memory model to represent a memory write operation in the physical memory," as recited in claim 14. *Isles Declaration*, ¶¶ 20-23, 28-29.

It was also shown with respect to claim 1, that the combination fails to teach or suggest, "replacing a portion of a description of the electronic circuit design with the lookup table, wherein the portion of the description relates to the physical memory, and wherein the lookup table in the description represents the physical memory." For at least the same reasons as set forth with respect to claim 1, it is respectfully submitted that the combination fails to teach or suggest, "replacing a portion of a description of the electronic circuit design with the memory model, wherein the portion of the electronic circuit design relates to the physical memory, and wherein the memory model in the description represents the physical memory." *Isles Declaration*, ¶¶ 20-23, 28-29; *Murgai*

Declaration, ¶¶ 7-15.

Thus, even if *Weems* and *Murgai* are combined as suggested by the Examiner, the resulting combination fails to teach or suggest each limitation of claim 14. Accordingly, it is respectfully submitted that claim 14 is patentable over the cited art. Claims 15-22 and 49 each ultimately depend from claim 14 and should be patentable for at least the same reasons.

Claims 29-33 and 51

Claim 29 recites a "processor readable storage medium having processor readable code embodied on the processor readable storage medium, the processor readable code for programming a processor to perform a method" comprising the steps recited in claim 1. Accordingly, it is respectfully submitted that claim 29 and claims 30-33 and 51, because of their dependency from claim 29, are patentable over the combination of *Weems* and *Murgai* for at least the same reasons as set forth with respect to claim 1.

Claims 34-41

Claim 34 includes the limitation "modeling a memory write operation of the electronic circuit design using a memory model." It was set forth with respect to claim 14 that the combination of *Weems* and *Murgai* fails to teach or suggest "modeling a memory write operation of the electronic circuit design in a memory model." Claim 34 further includes the limitation "replacing a portion of a description of the electronic circuit design with the memory model, wherein the portion of the description relates to the physical memory, and wherein the memory model in the description represents the physical memory," which is not taught or suggested by the combination of references as set forth with respect to claim 14. Accordingly, for at least the same reasons as set forth with respect to claim 14, Applicant asserts the claim 34 and claims 35-41 are patentable over the combination of references.

Claims 42-44

Claim 42 recites an apparatus including code to program a processor to perform the steps recited in claim 12. Accordingly, it is submitted that claim 42 is patentable over the art of record for at least the same reasons as claim 12. Claims 43 and 44 each ultimately depend from claim 42 and should be patentable for at least the same reasons.

D. The Combination of *Bayoumi* and *Murgai* Fails to Teach or Suggest each of the Limitations of Claim 23

Claim 23 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Bayoumi* in view of *Murgai*. Bayoumi, M. et al., *A Look-Up Table VLSI Design Methodology for RNS Structures Used in DSP Applications*, IEEE Transactions on Circuits and Systems, Vol. 34, Issue 6, June 1997, pp. 604-616 ("*Bayoumi*")

The combination of references fails to teach or suggest the following limitation of claim 23:

> ... creating a hardware description language description of the lookup table and a plurality of components of the electronic circuit design, wherein the hardware description language of the lookup table represents the physical memory of the electronic circuit design...

Bayoumi is not directed to and does not teach or suggest such a limitation. *Bayoumi* discloses a design methodology for Residue Number System (RNS) structures based on using look-up tables. *Bayoumi*, p. 606. The method described in *Bayoumi* develops a look-up table layout model and "selects the most efficient layout according to the design requirements by allowing the designer to control the area, time, or the configuration of the memory module required for implementing a modulo look-up table." *Id.* at a*bstract*, p. 604. *Bayoumi* is directed to the physical layout of memory modules which "are based on having several look-up tables connected together in the same package." *Id.* at p. 5. Thus, while *Bayoumi* discusses look-up tables, the discussion is limited to actual physical structures and the physical layout of memory modules including lookup tables. Nothing suggests a lookup table that serves as a model to "represent[] the physical memory of the electronic circuit design," in a hardware description language of the lookup table as recited in claim 23. *Isles Declaration*, ¶¶ 31-32.

The Examiner recognized that *Bayoumi* fails to disclose "the lookup table representing the physical memory with a description of the electronic design," as recited in claim 23 before the present amendment and cited *Murgai* for the missing limitation.

As set forth with respect to claim 1, however, *Murgai* fails to disclose "wherein the lookup table in the description represents the physical memory." In *Murgai*, a description is synthesized onto a lookup table architecture. The lookup table is the physical architecture onto which a design is synthesized. There is no suggestion of a "hardware description language of the lookup table represent[ing] the physical memory of the electronic design." In *Murgai*, the lookup table is a

physical architecture and does not represent "the physical memory of the electronic design," as recited in claim 23. *Isles Declaration,* ¶ 33; *Murgai Declaration,* ¶¶ 7-14, 17.

Because the combination of *Bayoumi* and *Murgai* fails to teach or suggest each of the limitations of claim 23, Applicant asserts that claim 23 is patentable over the cited art.

E. The Combination of *Bayoumi, Murgai,* and *Weems* Fails to Teach or Suggest Each of the Limitations of Claims 24-28

Claims 24-28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Bayoumi* in view of *Murgai*, and further in view of *Weems*. Because *Bayoumi, Murgai,* and *Weems*, either alone or in combination, fail to teach or suggest each of the limitations of claims 24-28, Applicant asserts that claims 24-28 are patentable over the cited art.

As discussed above with respect to claim 23, the combination of *Bayoumi* and *Murgai* fails to teach or suggest "creating a hardware description language description of the lookup table and a plurality of components of the electronic circuit design, wherein the hardware description language of the lookup table represents the physical memory of the electronic circuit design." As previously discussed with respect to claim 1 and 14, the combination of *Weems* and *Murgai* fails to teach or suggest "replacing a portion of a description of the electronic circuit design with the lookup table; wherein the portion of the description relates to the physical memory, and wherein the lookup table in the description represents the physical memory." Accordingly, it is respectfully submitted that the combination of all three references fails to teach or suggest, "wherein the hardware description language of the lookup table represents the physical memory of the electronic circuit design," as recited in claim 23.

Claims 24-28 each ultimately depend from claim 23 and should be patentable for at least the same reasons.

V. Conclusion

Based on the above amendments and these remarks, reconsideration and allowance of claims 1-51 is respectfully requested.

The Examiner's prompt attention to this matter is greatly appreciated. Should further questions remain, the Examiner is invited to contact the undersigned attorney by telephone.

Enclosed is a PETITION FOR EXTENSION OF TIME UNDER 37 C.F.R. § 1.136 for extending the time to respond up to and including today, August 25, 2004.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this document, including any fee for extension of time, which may be required.

Respectfully submitted,

Date: August 25, 2004

By: _____
David E. Cromer
Reg. No. 54,768

VIERRA MAGEN MARCUS HARMON & DENIRO LLP
685 Market Street, Suite 540
San Francisco, California 94105-4206
Telephone: (415) 369-9660
Facsimile: (415) 369-9665